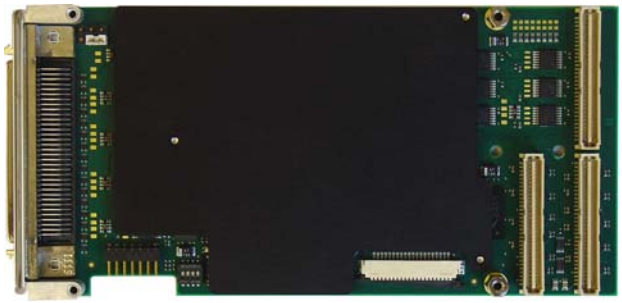
TPMC632 Reconfigurable FPGA with 64 TTL I/O / 32 Diff. I/O

Application Information

The TPMC632 is a standard single-width 32 bit PMC module providing a user configurable XC6SLX45T-2 or XC6SLX100T-2 Spartan-6 FPGA. The integrated Spartan-6's PCIe Endpoint Block is connected to a PCIe-to-PCI Bridge which routed to the PMC PCI Interface.



TPMC632-10R

The TPMC632-x0 has 64 ESD-protected TTL lines; the TPMC632-x1 provides 32 differential I/O lines using EIA-422 / EIA-485 compatible, ESD-protected line transceivers. The TPMC632-x2 provides 32 TTL and 16 differential I/Os. All lines are individually programmable as input, output or tri-state. The receivers are always enabled, which allows determining the state of each I/O line at any time. This can be used as read back function for lines configured as outputs. Each TTL I/O line has a pull resistor. The pull voltage level is selectable to be either +3.3V, +5V and additionally GND. The differential I/O lines are terminated by 120Ω resistors.

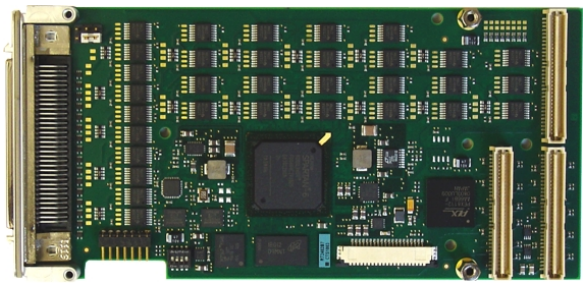
The FPGA is connected to a 128 Mbytes, 16 bit wide DDR3 SDRAM. The SDRAM-interface uses a hardwired internal Memory Controller Block of the Spartan-6.

The FPGA is configured by a platform flash or SPI flash. Both configuration flashes are in-system programmable. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx "ChipScope").

The TPMC632 provides front panel I/O via a HD68 SCSI-3 type connector and rear panel I/O via P14.

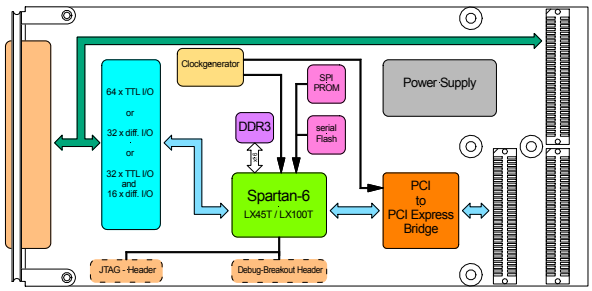
User applications for the TPMC632 with XC6SLX45T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com. The larger FPGA densities require a full licensed ISE Design Suite.

TEWS offers an FPGA Development Kit (TPMC632-FDK) which consists of well documented basic example design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TPMC632. It implements a DMA capable PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream.



TPMC632-10R without heat sink

Please note: The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available).



Software Support (TDRV015-SW-xx) for different operating systems is available.

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Technical Information

- Standard single-width 32 bit PMC module conforming to IEEE P1386.1
- PCI 2.1 compliant interface
- 3.3V and 5V PCI Signaling Voltage
- Board size: 149 mm x 74 mm
- TPMC632-1x: Xilinx XC6SLX45T-2 Spartan6 FPGA configured by serial Flash XCF16PFS
  TPMC632-2x: Xilinx XC6SLX100T-2 Spartan6 FPGA configured by serial Flash XCF32PFS
- Flash device is programmable via JTAG and in-system programmable
- FPGA clock options:
  - Local clock generator as source for the FPGA internal PLL
- 1 DDR3 SDRAM bank, 64M x 16 (128 MB)
- 32 Mbit SPI-EEPROM for User Data or FPGA configuration
- I/O lines
  - 64 TTL I/O (-10), 32 differential I/O (-11) or
    32 TTL I/O and 16 differential I/O (-12)
  - TTL signaling voltage (maximum current:
    +/-32mA) or EIA-422/-485 signaling level
  - direction individually programmable
- I/O access:
  64 I/O lines on HD68 front connector, parallel to
  up to 64 I/O lines on rear connector P14
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 G_B 20°C): tbd

Order Information

RoHS Compliant

TPMC632-10R	64 TTL I/O Lines, XC6SLX45T-2 Spartan-6 FPGA,128 MB DDR3
TPMC632-11R	32 Differential I/O Lines, XC6SLX45T-2 Spartan-6 FPGA,128 MB DDR3
TPMC632-12R	32 TTL and 16 Differential I/O Lines, XC6SLX45T-2 Spartan-6 FPGA,128 MB DDR3
TPMC632-20R	64 TTL I/O Lines, XC6SLX100T-2 Spartan-6 FPGA,128 MB DDR3
TPMC632-21R	32 Differential I/O Lines, XC6SLX100T-2 Spartan-6 FPGA,128 MB DDR3
TPMC632-22R	32 TTL and 16 Differential I/O Lines, XC6SLX100T-2 Spartan-6 FPGA,128 MB DDR3

Documentation

TPMC632-DOC	User Manual
TPMC632-ED	Engineering Documentation (includes TPMC632-DOC, Data Sheets and Constraints File)
TPMC632-FDK	FPGA Development Kit (includes TPMC632-ED and TPLD005 Example Design)

Accessories

TA900-10R	Program and Debug Box

Software

TDRV015-SW-25	Integrity Software Support (for the example design TPLD005 of the TPMC632-FDK)
TDRV015-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled) Software Support (for the example design TPLD005 of the TPMC632-FDK)
TDRV015-SW-65	Windows 7/XP/XPE/2000 Software Support (for the example design TPLD005 of the TPMC632-FDK)
TDRV015-SW-72	LynxOS Software Support (for the example design TPLD005 of the TPMC632-FDK)
TDRV015-SW-82	Linux Software Support (for the example design TPLD005 of the TPMC632-FDK)
TDRV015-SW-95	QNX 6 Software Support (for the example design TPLD005 of the TPMC632-FDK)

For other operating systems please contact TEWS.

Related Products

TA304	Cable Kit for modules with HD68 SCSI-3 type connector
TPIM003	PIM I/O Module with HD68 SCSI-3 type connector and special pin assignment

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