PMC I/O Module Standard

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1. Overview

1.1 Scope

This proposed standard defines a module intended to pair with a CMC compliant card via the 64 I/O signals defined on the Pn4/Jn4 connectors. To the extent possible, the proposed module reuses mechanical dimensions, hardware and connector definitions set forth in the CMC specification.

1.2 Purpose

The CMC specification provides for user defined I/O to exit the CMC through one or more 64 pin connectors. This user I/O is commonly employed to bring I/O to the rear of the system in order to augment or replace the I/O available on the CMC's bezel in the front of the system.

One of the primary benefits of using a CMC is that functionality can be added at the system integration level as opposed to being designed in onto the host board. For applications in which CMC user I/O must be brought to connectors on the system panel, it is desirable to have a generic module to allow this aspect of the CMC's functionality also to be integrated at the system level rather than the board level.

1.3 General Arrangement

The only current implementation of the CMC umbrella specification is the PCI Mezzanine Card (PMC). The definition of the PMC I/O Module (PIM) is based on their use on VME and CompactPCI transition boards. These transition boards hold similar form factors to their respective hosts with the exception of being shorter by 80mm. Consequently, the PIM is based on the standard length CMC but is 80mm shorter.

There are two CMC style 64 pin connectors on the PIM. One connector is dedicated to the 64 user I/O signals routed to it from the CMC. The second connector provides power and ground to the PIM. The second connector may also be used to bring host signals onto the PIM.

1.4 Dimensions

The intention is to reuse as much hardware and dimensional information as possible from the CMC specification. Stacking heights, connectors and bezel dimensions are unchanged from IEEE P1386. The CMC I/O envelope remains unchanged but the component envelope height limit is increased to better accommodate taller physical layer components (such as transformers, fuses, etc.).

2. References

The following publications are referenced within this document:

[1] IEEE P1386 Standard Mechanics for a Common Mezzanine Card Family: CMC

[2] IEEE P1386.1 Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC

3. Definitions, Abbreviations, and Terminology

3.1 Special Word Usage

Special word usage is unchanged from IEEE P1386.

3.2 Definitions

Host - refers to the board carrying the CMC.

Carrier - refers to the board carrying the PIM. The host and the carrier may be the same board.

Others definitions are unchanged from IEEE P1386.

3.3 Abbreviations

PIM - PMC I/O Module

Others abbreviations are unchanged from IEEE P1386.

4. PMC I/O Module Mechanics

4.1 PIM Size Designations and Sizes

Two different PIM sizes are defined. These sizes are defined in Table 1.

Table 1: PIM PCB Size Designations and Dimensions

Designation	Width	Depth
Single	74.0	69.0
Double	149.0	69.0

4.2 PIM Envelope

One notable departure from the CMC specification is in the definition of the component envelope space on the PIM and the carrier. It is envisioned that PIMs will typically be located on transition or connector break-out boards. Such carriers do not typically have large numbers of electronic components. This is taken advantage of to provide more room on the PIM for tall components by reducing the space allotted to the carrier. Thus it may be possible to use physical interface components on the PIM which may not fit on the CMC itself.

Note that the I/O envelope is identical to that on the CMC. This allows any connector arrangement on a CMC to be effortlessly replicated on the PIM.

The envelopes for a PIM and its carrier are detailed in Figure 1.

4.3 PIM Dimensions

The mechanical dimensions of the single and double PIM sizes are given in Figure 2 and Figure 3 respectively.

Note that standoff hole size is not defined. The size of these holes depends on how the standoffs are permanently attached to the PIM during assembly.

4.4 Connector Positioning, Orientation and Labeling

The PIM has two EIA E700 AAAB connectors identical to those used on a CMC. Likewise, pad layout is the same as that specified for a CMC.

It is expected that a PIM will normally have an orientation within a system opposite to that of its mating CMC. For instance, if a CMC is pointed bezel-wise towards the front of the system then the PIM will be pointing bezel-wise to the rear. To facilitate flow-through routing of the 64 user I/O signals, the Pn4 is moved to the opposite side of the PIM (to where Pn2 is located on a CMC) and is rotated by 180° from the orientation on the CMC. The label of Pn4 is kept to underscore the fact that it connected by the carrier and host to the Pn4 connector on the CMC.

The other connector is labelled Pn0 to emphasize that its use has no corresponding function in the CMC Pn1 through Pn4 connectors.

The relative positioning and orientation of the connectors on the PIM (and on the CMC for reference) are shown in Figure 4.

4.5 Power Consumption and Dissipation

Power drawn from the carrier shall not exceed the limits shown in Table 2. Under no circumstances should more than 0.5 amps be drawn through any single pin. The carrier should use bypass capacitors to ground on the PIM power pins.

Table 2: PIM Allowable Power Dissipation (In Watts)

Source	Single	Dual
Total	TBD	TBD
5V	TBD	TBD
3.3V	TBD	TBD
+12V	TBD	TBD
-12V	TBD	TBD

4.6 PIM Bezel and Stacking Heights

PIM stacking heights and bezel are unchanged from the CMC definitions.

Figure 1: Component Height Limits

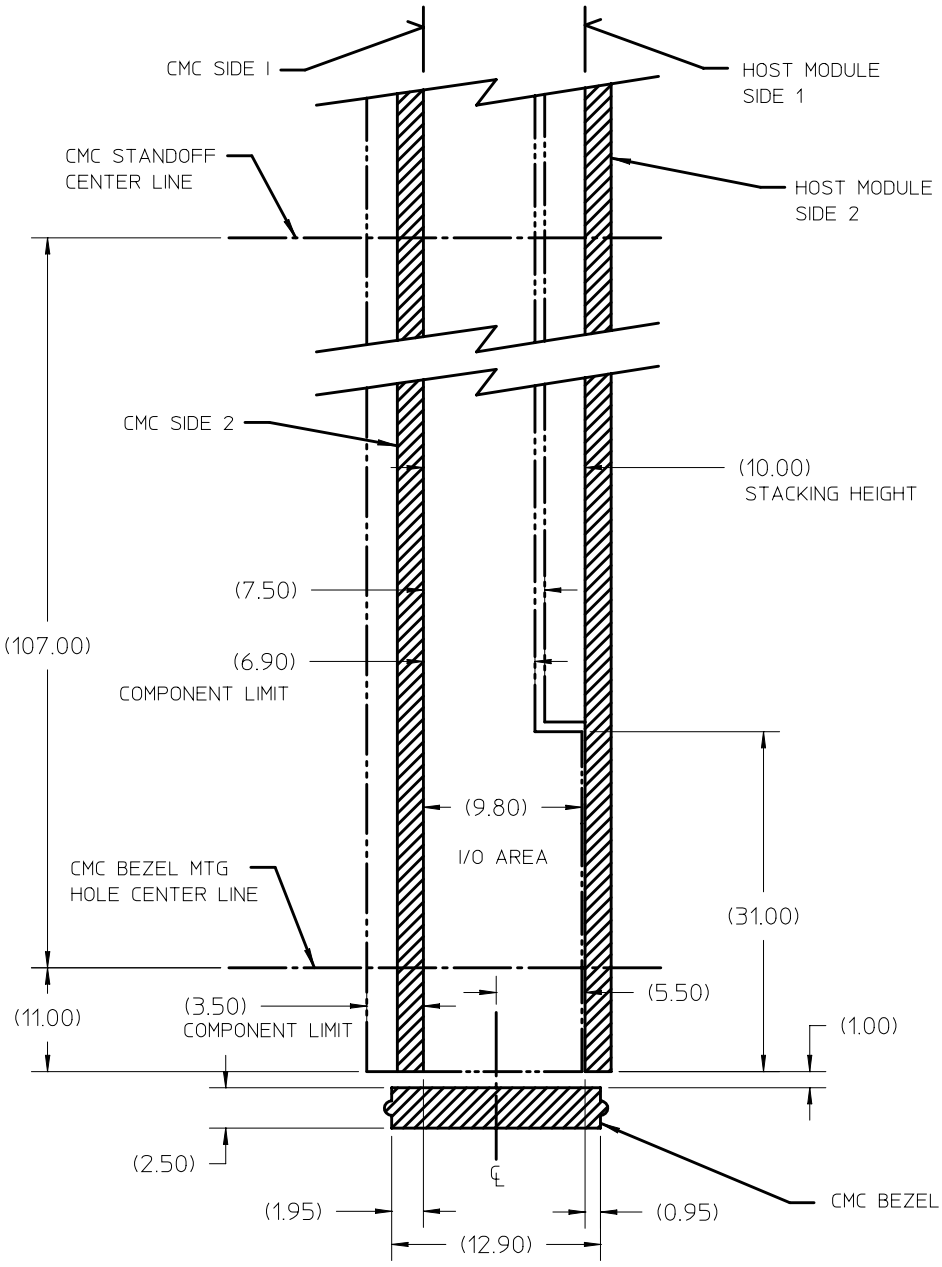


Figure 2: Single PIM

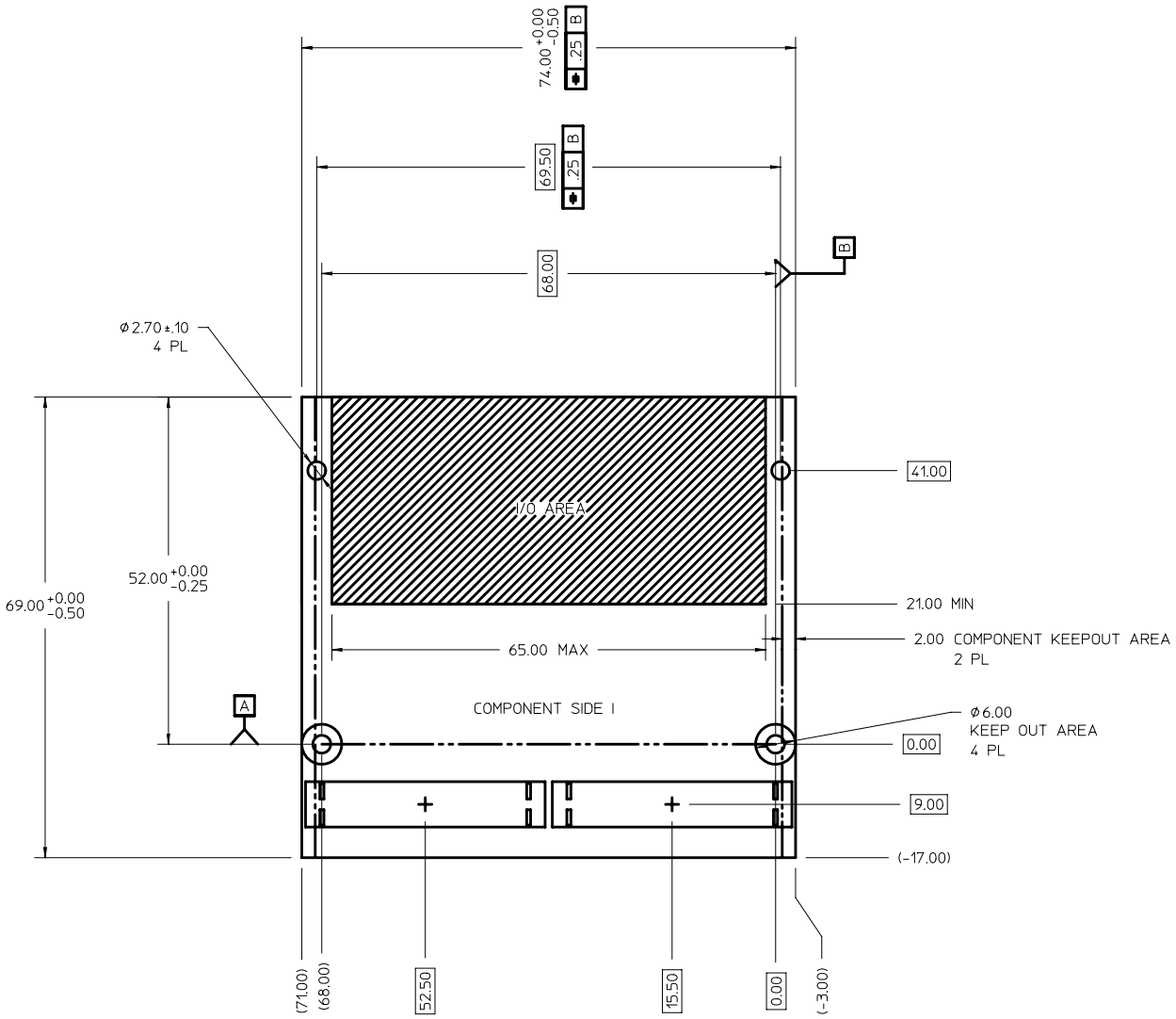


Figure 3: Double PIM

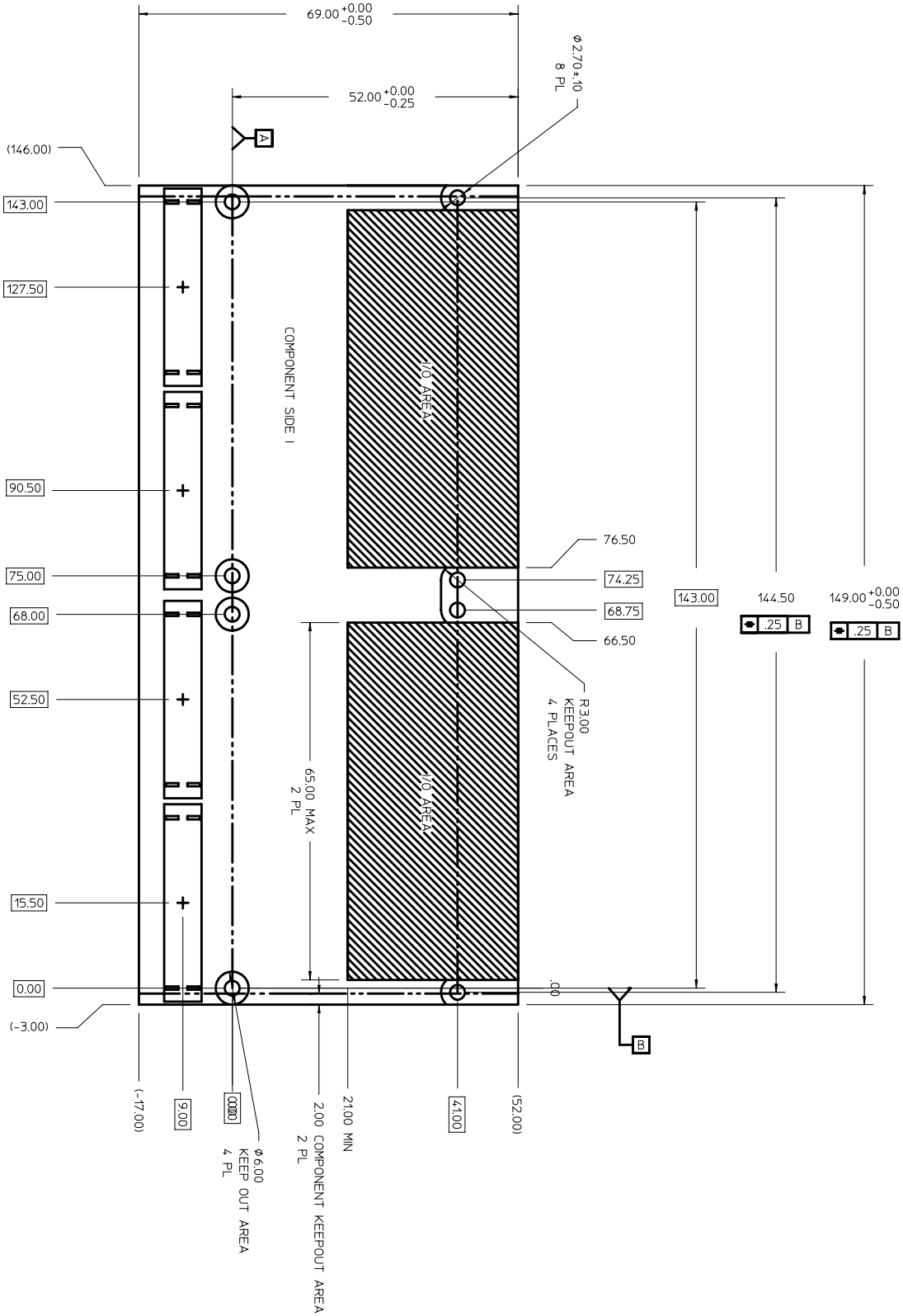
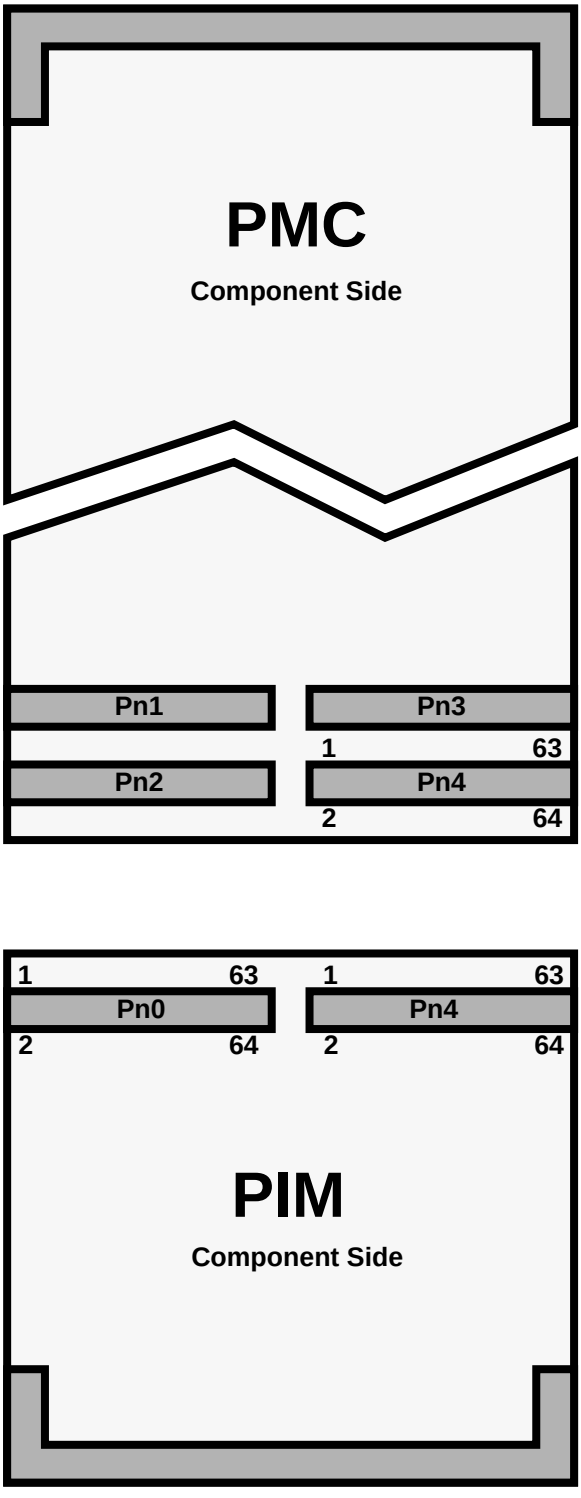


Figure 4: Positioning and Orientation of PIM Connectors



5. Carrier PIM Slot Mechanics

5.1 Carrier PCB Mechanics

VME or CompactPCI carrier boards can supprt either one or two PIM slots. The mechanics of these PCBs are defined in Figure 5 and Figure 6 for one or two slots, respectively.

5.2 Connectors

All host PIM connectors shall use the EIA E700 AAAB connector as required in the CMC specification. These connectors shall be referred to as the receptacle, or “Jn” connector. For single slot carriers, the connectors are labeled J10 and J14. For two slot carriers, the connectors are labeled J10, J14, J20 and J24. The host is required to supply both connectors.

Connector layout is the same as CMC, however position and orientation with regard to pin one location differs as shown in Figure 4.

5.3 Carrier Front Panel Opening and Filler

Size and placement of one or more PIM slot openings in the carrier front panel remain the same as the openings defined in the CMC specification. Consequently the PIM carrier may use filler panels used by CMC compliant hosts.

Figure 5: VME or CompactPCI Carrier for Single PIM

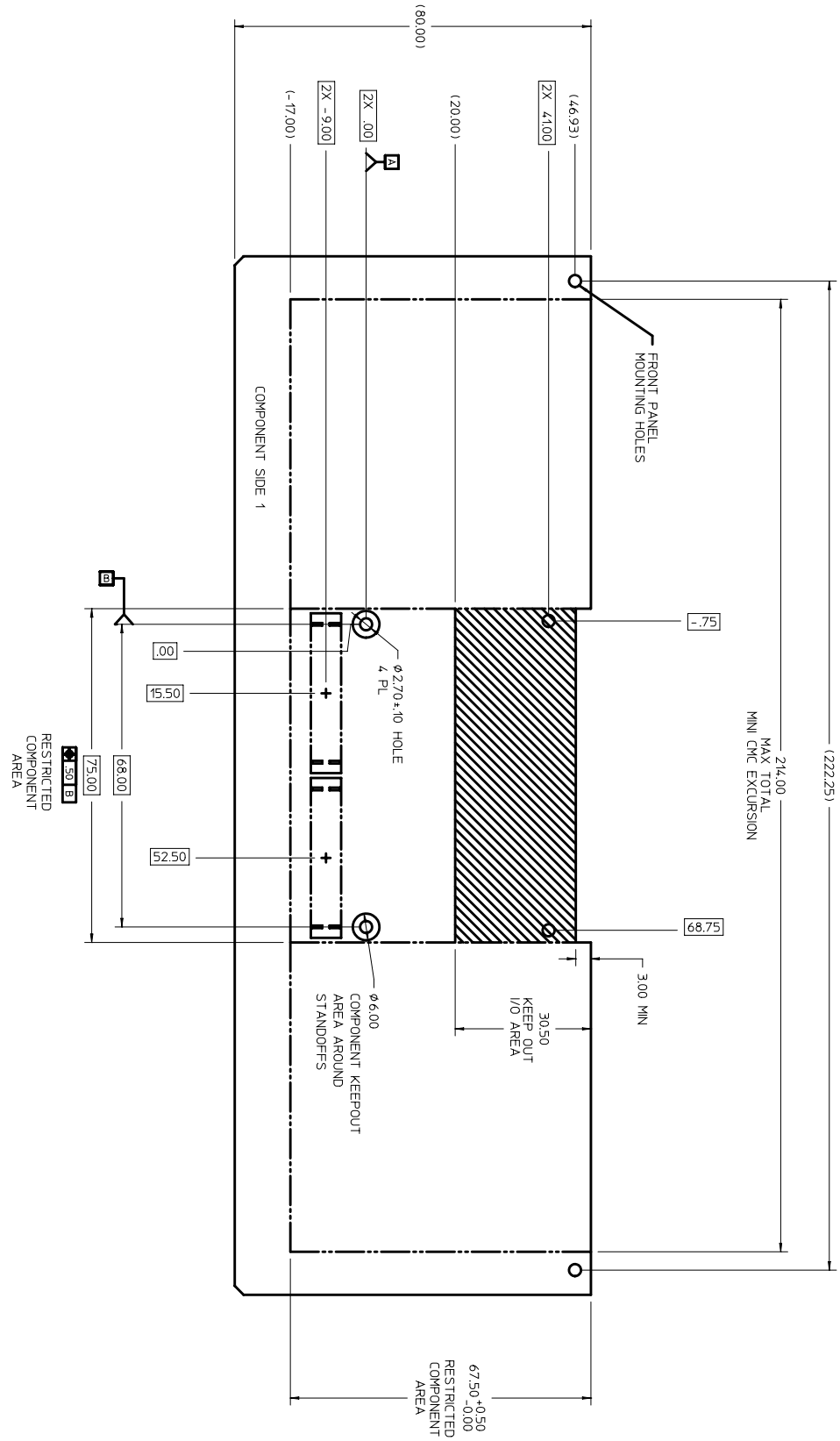
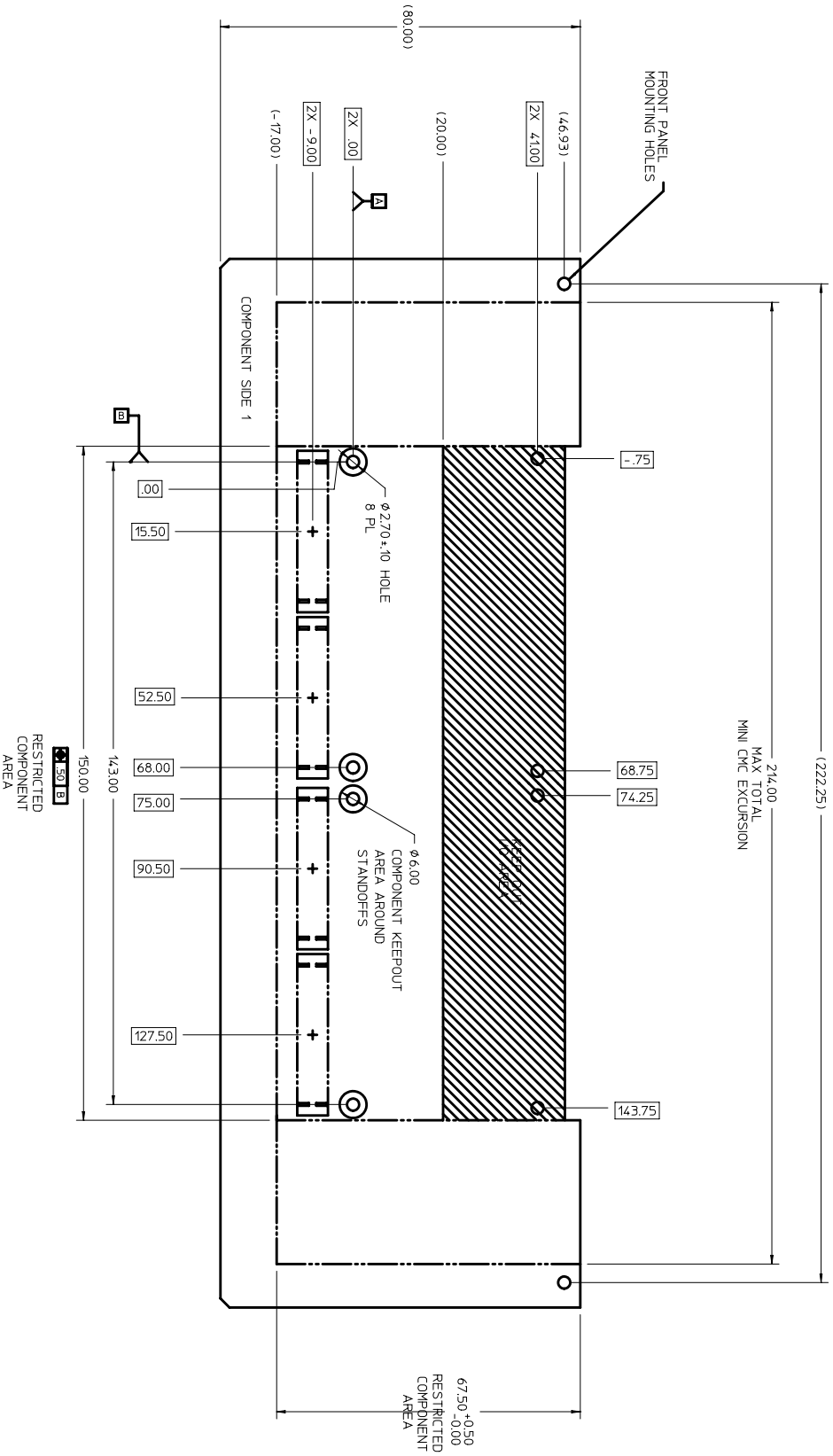


Figure 6: VME or CompactPCI Carrier for Double or Two Single PIMs



6. Electrical and Logical Layers

6.1 Connector Utilization

There are two 64 pin connectors on the PIM. One connector (Pn4) is reserved for CMC I/O and is directly mapped to the Pn4 connector on the CMC with which the PIM is paired. The second connector (Pn0) supplies power and logic ground to the PIM, and may optionally be used to bring host I/O signals onto the PIM.

The carrier is required to provide both connectors and to supply power and ground through the Jn0 connector as defined in Table 3. The carrier is not required to connect any of the signal pins on Jn0.

6.1.1 CMC I/O Connector

The Pn4/Jn4 connectors are referred to as CMC I/O connectors. The signals on the PIM Pn4 connector are directly mapped to the CMC Pn4 connector. This means Pn4-1 on the CMC is routed to Pn4-1 on the PIM, CMC Pn4-2 to PIM Pn4-2, and so forth up to Pn4-64. How these signals are used is determined entirely by the CMC and PIM design.

Note the Pn4 connector is in a different position and orientation on the PIM than on the CMC.

6.1.2 Host I/O Connector

The presence of the PIM slot on the carrier may displace host I/O from the carrier front panel. If no CMC is installed on the host (or the CMC does not require the use of a PIM) then the PIM slot may be reclaimed for host I/O. To support this the carrier may connect I/O signals to the Jn0 connector. A PIM which supports special host I/O instead of CMC I/O may be referred to as a “host I/O module”. Whereas a PIM is expected to function in any PIM slot, a host I/O module will only function in a PIM slot with the special connections it requires.

If the host I/O module includes the Pn4 connector, it must not make any connections to the pins to prevent contention with a CMC which may be installed on the host.

6.2 PIM Connector Pinout

The pin assignments and signal names required for the PIM are given in Table 3.

Table 3: PIM Connector Pin Assignments

Pn0/Jn0				Pn4/Jn4			
Pin	**Signal Name**	**Signal Name**	**Pin**	**Pin**	**Signal Name**	**SignalName**	**Pin**
1	Signal	+12V	**2**	**1**	I/O	I/O	**2**
3	Signal	Signal	**4**	**3**	I/O	I/O	**4**
5	+5V	Signal	**6**	**5**	I/O	I/O	**6**
7	Signal	Signal	**8**	**7**	I/O	I/O	**8**
9	Signal	+3.3V	**10**	**9**	I/O	I/O	**10**
11	Signal	Signal	**12**	**11**	I/O	I/O	**12**
13	GND	Signal	**14**	**13**	I/O	I/O	**14**
15	Signal	Signal	**16**	**15**	I/O	I/O	**16**
17	Signal	GND	**18**	**17**	I/O	I/O	**18**
19	Signal	Signal	**20**	**19**	I/O	I/O	**20**
21	+5V	Signal	**22**	**21**	I/O	I/O	**22**
23	Signal	Signal	**24**	**23**	I/O	I/O	**24**
25	Signal	+3.3V	**26**	**25**	I/O	I/O	**26**
27	Signal	Signal	**28**	**27**	I/O	I/O	**28**
29	GND	Signal	**30**	**29**	I/O	I/O	**30**
31	Signal	Signal	**32**	**31**	I/O	I/O	**32**
33	Signal	GND	**34**	**33**	I/O	I/O	**34**
35	Signal	Signal	**36**	**35**	I/O	I/O	**36**
37	+5V	Signal	**38**	**37**	I/O	I/O	**38**
39	Signal	Signal	**40**	**39**	I/O	I/O	**40**
41	Signal	+3.3V	**42**	**41**	I/O	I/O	**42**
43	Signal	Signal	**44**	**43**	I/O	I/O	**44**
45	GND	Signal	**46**	**45**	I/O	I/O	**46**
47	Signal	Signal	**48**	**47**	I/O	I/O	**48**
49	Signal	GND	**50**	**49**	I/O	I/O	**50**
51	Signal	Signal	**52**	**51**	I/O	I/O	**52**
53	+5V	Signal	**54**	**53**	I/O	I/O	**54**
55	Signal	Signal	**56**	**55**	I/O	I/O	**56**
57	Signal	+3.3V	**58**	**57**	I/O	I/O	**58**
59	Signal	Signal	**60**	**59**	I/O	I/O	**60**
61	-12V	Signal	**62**	**61**	I/O	I/O	**62**
63	Signal	Signal	**64**	**63**	I/O	I/O	**64**

6.3 PMC I/O Signal Routing

In general, the signals routed from the CMC Pn4 connector to the PIM Pn4 connector should be as short as possible, be approximately matched in length and have as few impedance mismatches as possible.

For VME and CompactPCI systems, the carrier will map the PIM Jn4 connector onto the backplane connector(s) in the exact same manner as the host maps the CMC Jn4 connector onto the backplane connector(s).

6.4 Host I/O Signal Routing

Host I/O is specific to the host. It is expected that the manufacturer of the carrier will also manufacture any host I/O modules which may be accommodated by the carrier. Requirements for host I/O signal routing must be determined by that manufacturer.

Higher speed signals should avoid using the +12V or -12V power pins as a signal return path. These power sources are generally not implemented with a plane and although it is recommended that the carrier bypass these voltages to ground near the connector, it is not required.