Processor PMC Standard

For Processor PCI Mezzanine Cards

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1 Overview

1.1 Scope

This proposed standard incorporates a set of extensions to the IEEE P1386.1 PMC ("PCI Mezzanine Card") standard which will: a) update the PMC interface to comply with the PCI interface standard. b) allow the creation of a new class of CPU based PMC cards referred to in this specification as Processor PMC (PPMC) cards. The proposed standard retains electrical signaling compatibility with existing PMC cards.

The complete physical (mechanical) and the environmental layers are retained as specified in the IEEE P1386 CMC ("Common Mezzanine Card") standard except as noted in this document.

1.2 Purpose

In recent years, the accelerated speeds of processor and external cache busses, increased levels of semiconductor integration, coupled with the desire to quickly upgrade systems to newer processor or memory technologies present the possibility of creating a complete processor and memory subsystem on a PMC card. Unfortunately, the current PMC specification is oriented to the expansion or I/O controller architecture of PCI. It does not define the necessary signals required to implement PCI based system boards (or motherboards) with a PMC as the main processor. These signals include:

- Interrupt handling
- 66 MHz PCI operation
- Confined physical space due to single slot VME/CompactPCI environments

The system board features of the PPMC specification are implemented by redefining some existing pins and by adding new definitions to previously reserved or obsolete pins. Additionally, the PPMC specification extends the height restriction on side two of the existing PMC standard in order to accommodate the following large devices:

- Heat-sink/fan-sink cooled processors.
- SODIMM-socketed memory modules.
- Connectors and/or power supplies.

1.3 General Description

PPMC cards are used where modular attachment of a processor is desired. These processor PMC cards may be used in conjunction with PMC I/O cards, traditional PCI cards, or with directly attached PCI components. As such, PPMC cards increase the modularity of a computer system and thus complement, rather than compete with, the existing family of PMC cards.

PPMC cards must electrically operate with existing carrier boards (or motherboards); that is, while the carrier board may be redesigned to take advantage of the enhanced functions that are offered by this standard, such a redesign must not be a requirement to insure proper operation. Indeed, PPMC cards must be specifically enabled to operate as master/host CPUs; otherwise, such cards revert to traditional PMC modes, operating as intelligent slave/target processor boards.

1.4 Dimensions

All mechanical dimensions are as specified in P1386, except where noted within this document. All dimensions are in millimeters.

1.4 Monarch and Non-monarch PPMCs

Two types of PPMCs are defined which might also be described as master or host and slave or target. While generally understood, these definitions can become confusing, especially when the clock generator and PCI arbiter do not reside on the PPMC card. With hopes of minimizing confusion with other

architectures and definitions, the terms monarch and non-monarch will be used in this document. The monarch is defined as the main PCI bus PPMC (or CPU); the one that performs PCI bus enumeration at power-up and often acts as an interrupt handler. A Non-monarch is therefore not the main CPU, does not perform PCI bus enumeration after power-up and is an interrupt generator. The MONARCH signal defines a PPMC as a being monarch or non-monarch. Naturally there must only be one monarch per system while there can be as many non-monarchs as the electrical interface on the carrier card will support. The optional EREADY signal is an output of non-monarch PPMCs that indicates it has completed its on-board initialization and can respond to PCI bus enumeration by the monarch via configuration cycles.

1.4 Optional Second PCI Agent

The PMC specification defines one PCI load per PMC. In some cases it is attractive to allow two loads on a PPMC. The second load on a PPMC monarch is referred to as the optional second PCI agent. The non-monarch PPMCs may include the optional second PCI agent. In order to support this additional PCI agent, an IDSEL select signal and RQST/GNT arbitration pair have also been added. Since an extra CLK signal is not provided for this second PCI device, use special care with this area of the design.

2 References

The following publications are used in conjunction with this standard:

[1] IEEE P1386/Draft 2.0 Standard Mechanics for a Common Mezzanine Card Family: CMC

[2] IEEE P1386.1/Draft 2.0 Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC

[3] PCI Local Bus Specification, Revision 2.2

3 Definitions, Abbreviations, and Terminology

3.1 Special Word Usage

Carrier defines the board on which the PPMC is installed; it may support one Monarch and/or multiple Non-monarch PPMC sites.
Monarch defines the main PPMC on the local PCI bus; it performs enumeration on that bus after power-up and is very likely an interrupt handler.
Non-monarch defines the additional PPMCs on the local PCI bus; they do not perform enumeration on that bus after power-up.
PPMC describes a Processor PMC; PPMCs are defined in this document.
Optional second PCI agent describes the one allowed additional PCI device on a Processor PMC; an ethernet port is often identified as a popular optional second PCI agent.

Others are unchanged from IEEE P1386.1

4 Mechanics and Compliance

4.1 Conformance

The PPMC specification remains in conformance with the IEEE P1386 / P1386.1 draft standards whenever possible; however, those specifications are oriented to low-power, low-profile PCI peripheral cards which are designed to fit into a height allowed by a single slot of a VME chassis. This results in a maximum component height of between 2.50-5.50 mm on side two (depending upon the positioning of the PCB).

This restriction is not suitable or required for Processor PMC purposes, so the PPMC specification adds a mechanical dimension term to describe expansion in the height (z) category. The PMC specification uses the terms “single” and “double” to describe different widths, and the term “extended” to describe extended length. Similarly, the PPMC specification uses the term “tall” to describe PMC cards, which provide additional height.

The PPMC standard adds an additional 20 mm (the height required by one additional VME or CompactPCI slot) to the total height of side two:

Table 1: PPMC Card Height Designations and Dimensions

Type	Standoff/ Stacking Height	Side 1 Component Height	Side 2 Component Height	Notes
Standard	8.00	2.70	5.50	
"	9.00	3.70	4.50	
"	10.00	4.70	3.50	Preferred height for standard cards
"	11.00	5.70	2.50	
Tall	8.00	2.70	25.50	
"	9.00	3.70	24.50	
"	10.00	4.70	23.50	Preferred height for tall cards
"	11.00	5.70	22.50	

4.2 PMC Voltage keying

No change from IEEE P1386.1

4.3 Connector Configurations

No change from IEEE P1386.1

4.4 Power Consumption, heat Dissipation and Air Flow

The PMC specification limits power consumption and heat dissipation due to the close vertical spacing. As the PPMC specification adds the option of additional height, this in turn supports additional power and heat dissipation. This section supersedes Table 4-3 in the IEEE 1386 CMC specification.

Since the total amount of power and cooling are critical to the overall system design, it is up to the manufacturer to define the power required by the PMC or the power that the carrier can supply to the PPMC site(s). Under no circumstances may the maximum rated power or current demands exceed the rated limit of 0.50A/pin. The PPMC manufacturer must indicate the total power required from the different power sources (+5V, +3.3V, ± 12V) and from each connector (Pn1, Pn2, and optionally Pn3) if applicable.

Observation: While specifying PPMC power dissipation limits is difficult and possibly overly restrictive, the use of a standard length, single wide, standard height PPMC with over 12 watts or tall PPMC with over 25

watts power may require additional design and cooling considerations. Given this new approach to power requirements, Table 4-3 in CMC P1386/Draft 2.0 is not updated.

4.5 Electromagnetic Compatibility

No change from IEEE P1386.1

4.6 Shock and Vibration

No change from IEEE P1386.1

4.7 Environmental

No change from IEEE P1386.1

4.8 MTBF

No change from IEEE P1386.1

5 Electrical and Logical layer

5.1 Connector Utilization

No change from IEEE P1386.1

5.2 PMC/PPMC Connector ~~Pinout~~ Signal Summary

Changes from IEEE P1386.1 are shaded and described in this specification.

Notes: # = Active Low
PUP = Pull Up
PCI-xx = Reserved Pin xx in PCI Spec, Rev 2.2
PDN = Pull Down

Table 3: Connector ~~Pinout~~ Signal Summary

Pn1/Jn1 32 Bit PCL				Pn2/Jn2 32 Bit PCL			
Pin #	**Signal Name**	**Signal Name**	**Pin #**	**Pin #**	**Signal Name**	**Signal Name**	**Pin #**
1	TCK <B2>	-12V	2	1	+12V	TRST# <A1>	2
3	Ground	INTA# <A6>	4	3	TMS <A3>	TDO <B4>	4
5	INTB# <B7>	INTC# <A7>	6	5	TDI <A4>	Ground	6
7	PRESENT# <B9>	+5V	8	7	Ground	PCI-Res <A9>~~P~~	8
9	INTD# <B8>	PCI-Res <B14>~~-B~~	10	9	PCI-Res <B10>~~P~~ ~~B10~~	PCI-Res <A11>~~P~~ ~~A11~~	10
11	Ground	3.3Vaux <A14>	12	11	PUP <A14>	+3.3V	12
13	PCICLK <B16>	Ground	14	13	RST# <A15>	PDN	14
15	Ground	GNT# <A17>	16	15	+3.3V	PDN	16
17	REQ# <B18>	+5V	18	17	PME# <A19>	Ground	18
19	V(I/O)	AD[31] <B20>	20	19	AD[30] <A20>	AD[29] <B21>	20
21	AD[28] <A22>	AD[27] <B23>	22	21	Ground	AD[26] <A23>	22
23	AD[25] <B24>	Ground	24	23	AD[24] <A25>	+3.3V	24
25	Ground	C/BE[3]# <B26>	26	25	IDSEL <A26>	AD[23] <B27>	26
27	AD[22] <A28>	AD[21] <B29>	28	27	+3.3V	AD[20] <A29>	28
29	AD[19] <B30>	+5V	30	29	AD[18] <A31>	Ground	30
31	V(I/O)	AD[17] <B32>	32	31	AD[16] <A32>	C/BE[2]# <B33>	32
33	FRAME# <A34>	Ground	34	33	Ground	IDSELB	34
35	Ground	IRDY# <B35>	36	35	TRDY# <A36>	+3.3V	36
37	DEVSEL# <B37>	+5V	38	37	Ground	STOP# <B38>	38
39	Ground	LOCK# <B39>	40	39	PERR# <B40>	Ground	40
41	PCI-Res <A41>~~-A~~	PCI-Res <A40>~~P~~ ~~A41~~	42	41	+3.3V	SERR# <B42>	42
43	PAR <A43>	Ground	44	43	C/BE[1]# <B44>	Ground	44
45	V(I/O)	AD[15] <A44>	46	45	AD[14] <B45>	AD[13] <A46>	46
47	AD[12] <B47>	AD[11] <A47>	48	47	M66EN	AD[10] <B48>	48
49	AD[09] <A49>	+5V	50	49	AD[08] <B52>	+3.3V	50
51	Ground	C/BE[0]# <A52>	52	51	AD[07] <B53>	REQB#	52
53	AD[06] <A54>	AD[05] <B55>	54	53	+3.3V	GNTB#	54
55	AD[04] <A55>	Ground	56	55	PMC-RSVD	Ground	56
57	V(I/O)]	AD[03] <B56>	58	57	PMC-RSVD	EREADY	58
59	AD[02] <A57>	AD[01] <B58>	60	59	Ground	RESETOUT#	60
61	AD[00] <A58>	+5V	62	61	ACK64# <B66>	+3.3V	62
63	Ground	REQ64# <A60>	64	63	Ground	MONARCH#	64

Notes:

a) *For future PCI compatibility, this specification maps the ~~previous "PCI Reserved"~~PMC signals to specific signals in the PCI Local Bus Specification Revision 2.2. The PCI signal (for example B2) that defines the PMC signal (for example TCK) in the above table is abbreviated as <B2>.*

b) *This specification only redefines PMC reserved signals; no PCI reserved signals have been used.*

c) *PCI Spec Rev 2.2 redefined the following signals: PCI reserved A40 & A41, 3.3Vaux, and PME.*

d) *Pn3/Jn3 and Pn4/Jn4 are unchanged.*

e) *Pullups and/or pulldowns defined by the PCI Bus Specification and not defined in this specification shall reside on the carrier.*

5.2.1 PRESENT#

New signal not defined in IEEE P1386.1

The PRESENT# signal is connected to ground on a PPMC card to indicate to a carrier that a PMC card has been installed. PRESENT# replaces the BUSMODE1# pin, which on PMC cards is a more involved method of querying both the presence and protocol of a PMC card using signals on the BUSMODE[2:4]# pins. The PPMC specification replaces this complicated protocol detection with a simple present/not-present indicator, as PCI operation is mandated.

Observation for carrier support of both PMCs and PPMCs: In order to maintain compatibility with previous BUSMODE[2:4]# designs and interoperability with current PMC cards, PPMC-capable carriers must provide weak pullups or pulldowns (10K ohm pull up, 10~~1~~K ohm pull down) on the PUP and PDN signals.

5.2.2 MONARCH#

New signal not defined in IEEE P1386.1

The MONARCH# signal allows the carrier to enable the monarch features of a PPMC card. If the MONARCH# is connected to ground, then the PPMC must provide PCI bus enumeration and interrupt handling. If the signal is disconnected and allowed to float high, the card must revert to standard PMC I/O card behavior. The MONARCH# signal must be connected to a weak pullup (10K Ω) on the PPMC card to insure that a floating input is recognized. The MONARCH# signal redefines the behavior of the interrupts, as follows:

Table 4 : MONARCH# Reconfiguration

MONARCH#	Mode	Signal	Function	Description
Float	Standard PMC	INT[A:D]#	INT[A:D]#	Interrupt typically is an output.
Ground	PPMC Monarch	INT[A:D]#	INT[A:D]#	Interrupt typically is an input.

The monarch must provide the ability to respond to interrupt signals on the INT[A:D]# signals (software is responsible for handling interrupts). The interrupt signals are bussed in parallel, so interrupt handling can be easily re-assigned or partitioned among several PPMC cards.

The monarch functions are defined to exist on the designated card during and immediately after the release of the PCI reset signal. Changes thereafter to the interrupt handling are matters for systems architecture and software.

Interoperability with current PMC cards is preserved, as MONARCH# uses a previously unused pin.

Table 5 : MONARCH# Interoperability

PMC	Attachment	Effects
P1386.1 (Current)	Carrier (Current)	No effect – current standards.
PPMC (New)	Carrier (Current)	MONARCH floats, so PPMC is not configured as a monarch.#
P1386.1 (Current)	Carrier (New)	MONARCH# connects to unused pin; no electrical conflict
PPMC (New)	Carrier (New)	MONARCH# may be used to enable system control functions.

5.2.3 M66EN

New signal not defined in IEEE P1386.1

Optional operation of the PCI bus at 66MHz is a new addition to the PCI specification. While the PCI specification has new signal definitions that have been modified to support 66 MHz operation, these are backward compatible with 33 MHz operation and have no adverse effect on existing devices. To accomplish this, one of the ground pins, pin B49, of the PCI connector has been redefined such that 66 MHz-capable devices disconnect this pin and allow it to float or control it via an open-drain output). If any non-66 MHz device is present, the M66EN signal will be asserted low and global 33 MHz operation is enforced.

This specification places the function of M66EN on Pn2 pin 47. This satisfies the requirement of replacing an existing ground pin, attaining the backward compatibility needed, and also conforms well with the relative placement of PMC connector signals and PCI connector signals.

Table 6 : M66EN Interoperability

PMC	Attachment	Effects
P1386.1 (Current)	Carrier (Current, 33MHz)	No effect – current standards.
PPMC (New)	Carrier (Current, 33MHz)	M66EN is grounded, 66MHz operation is prevented.
P1386.1 (Current)	Carrier (New, 66MHz)	M66EN is grounded, 66MHz operation is prevented.
PPMC (New)	Carrier (New, 66MHz)	66 MHz operation is allowed if all PMCs allow M66EN to float..

5.2.4 IDSELB

New signal that is similar to IDSEL# but is not defined in IEEE P1386.1

The IDSELB signal is an optional input signal. It is used to select an optional second PCI agent. If PPMC with second agent is to be compatible with standard PMC carriers, then IDSELB should have a weak (~~1K~~ 10K ohm) pulldown on PPMC and GNTB should have a weak (10K ohm) pullup on PPMC.

5.2.5 REQB#

New signal that is similar to REQ# but is not defined in IEEE P1386.1

The REQB# output signal is a request issued by the optional second PCI agent requesting the ownership of the PCI bus.

5.2.5 GNTB#

New signal that is similar to GNT# but is not defined in IEEE P1386.1

The GNTB# input signal is a grant issued to the optional second PCI agent which requested ownership of the PCI bus via the corresponding REQB# signal.

5.2.6 INT[A:D]#

Some changes from IEEE P1386.1 to allow bi-directional signals

The INT[A:D]# signals are open-drain lines which may be driven by any PCI agent. Originally these signals were outputs only but they must now be bi-directional. For PPMC cards these signals become inputs since it is necessary to respond to interrupt signals on these lines. When a Monarch PPMC is properly configured, it will reconfigure its INT[A:D]# outputs as inputs and will handle detected interrupts.

The INT[A:D]# pin assignments will not cause backward compatibility issues. The interoperability details are summarized in the following table:

Table 7 : INT[A:D]# Interoperability

PMC	Attachment	Effects
P1386.1 (Current)	Carrier (Current)	No effect – current standards.
PPMC (New)	Carrier (Current)	PPMC cannot be a configured as a monarch, so interrupts are not Handled (card may optionally assert interrupts).
P1386.1 (Current)	Carrier (New)	PPMC cannot be configured as a monarch, so interrupts are not handled (card may optionally assert interrupts).
PPMC (New)	Carrier (New)	One PPMC card is designated as monarch, and provides Interrupt handling.

NOTE: The open-drain outputs require a pull up to properly stabilize the signal; this pull up must be provided on the carrier. The mapping of the optional second PCI agent follows.

Table 8 : Interrupt mapping for optional second PCI agent

Second Agent INT	PMC INT
INTA#	INTB#
INTB#	INTC#
INTC#	INTD#
INTD#	INTA#

5.2.7 RST#

No change from IEEE P1386.1

Note that the carrier board is still expected to generate the reset signal as an input to all PPMC cards. PPMC cards do not create this signal since RST# is an input to the PPMC. A pull up must be provided on the carrier.

5.2.8 RESET_OUT#

New signal not defined in IEEE P1386.1

The RESET_OUT# signal is an open drain output of the PPMC that becomes an input to the reset logic residing on the carrier card. This optional signal supports a reset button or other reset source on the PPMC. To avoid reset loops, RST# must not be used to generate RESETOUT#. Timing for the active RESETOUT# signal pulse width is like that described in the PCI Local Bus Specification for RST#.

5.2.9 CLK

Some changes from IEEE P1386.1 to allow 66 MHz operation

Note that the carrier board is still expected to generate the PCI clock signal as an input to all PPMC cards. PPMC cards use this PCI clock input to generate all clocks required by the PPMC. Additionally, a 66 MHz capable carrier must examine the M66EN signal to determine whether 33 MHz operation is possible.

Observation: The PPMC should present 1 load to the carrier generated CLK driver, even when an optional second PCI agent is used. Otherwise take special care when designing the PPMC CLK circuitry.

5.2.10 EREADY

New signal not defined in IEEE P1386.1

The EREADY signal is an open drain output of non-monarch PPMCs that indicates the non-monarch PPMC has completed its on-board initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. The EREADY signal is an input to the monarch PPMC that indicates all non-monarch PPMCs have completed their on-board initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. The carrier provides a weak pull up (5K ohm) for EREADY. The PPMC should also provide a weak pull up (105K ohm) to maintain software compatibility with carrier boards that don't implement this signal.

5.2.11 Comparison of Pin Usage -- Traditional PMC to Monarch and Non-Monarch PPMC

Notes: # = Active Low
PUP = Pull Up PDN = Pull Down
M = Monarch PPMC NM = Non-Monarch PPMC
✓ = Required R = Recommended O = Optional

Table 9 : PMC and PPMC Differences

Pin	PMC	NM	M	PPMC	Change
Pn1-4	INTA#	R	✓	INTA#	Output; may be output or input on PPMC.
Pn1-5	INTB#	R	✓	INTB#	Output; may be output or input on PPMC.
Pn1-7	BUSMODE1#	✓	✓	PRESENT#	Output; grounded on PPMC cards.
Pn1-6	INTC#	R	✓	INTC#	Output; may be output or input on PPMC.
Pn1-9	INTD#	R	✓	INTD#	Output; may be output or input on PPMC.
P12-11	BUSMODE2#	✓	✓	PUP	Weak pull-up on carrier to maintain BUSMODE compatibility.
Pn2-14	BUSMODE3#	✓	✓	PDN	Weak pull-down on carrier to maintain BUSMODE compatibility.
Pn2-16	BUSMODE4#	✓	✓	PDN	Weak pull-down on carrier to maintain BUSMODE compatibility.
P12-11	BUSMODE2#	✓	✓	PUP	Weak pull up on carrier to maintain BUSMODE compatibility.
Pn2-14	BUSMODE3#	✓	✓	PDN	Weak pull down on carrier to maintain BUSMODE compatibility.
Pn2-16	BUSMODE4#	✓	✓	PDN	Weak pull down on carrier to maintain BUSMODE compatibility.
Pn2-34	PMC-RSVD	O	O	IDSELB	ID Select for second agent on PPMCs; Recommend weak pull down on PPMC.
Pn2-47	GROUND	✓	✓	M66EN	Ground/output; floating on 66-MHz PPMC cards, grounded on all other cards (PMC or PPMC).
Pn2-52	PMC-RSVD	O	O	REQB#	Request for second agent on PPMCs.
Pn2-54	PMC-RSVD	O	O	GNTB#	Grant for second agent on PPMCs; Recommend weak pull up on PPMC.
Pn2-58	PMC-RSVD	O	O	EREADY	Indicates NM PPMC is ready to respond to PCI bus enumeration.
Pn2-60	PMC-RSVD	O	O	RESETOUT#	Output; reset signal to the carrier card; drives reset logic on the carrier card.
Pn2-64	PMC-RSVD	✓	✓	MONARCH#	Input; MONARCH# selects PPMC PCI Bus enumeration and interrupt controllers after reset.

Notes:
a) Table 3 maps previous generic "PCI-Reserved" signals to specific PCI signals in the PCI bus local specification.
b) PCI Spec Rev 2.2 also redefined the following signals listed in Table 3: PCI reserved A40 & A41, 3.3Vaux, and PME

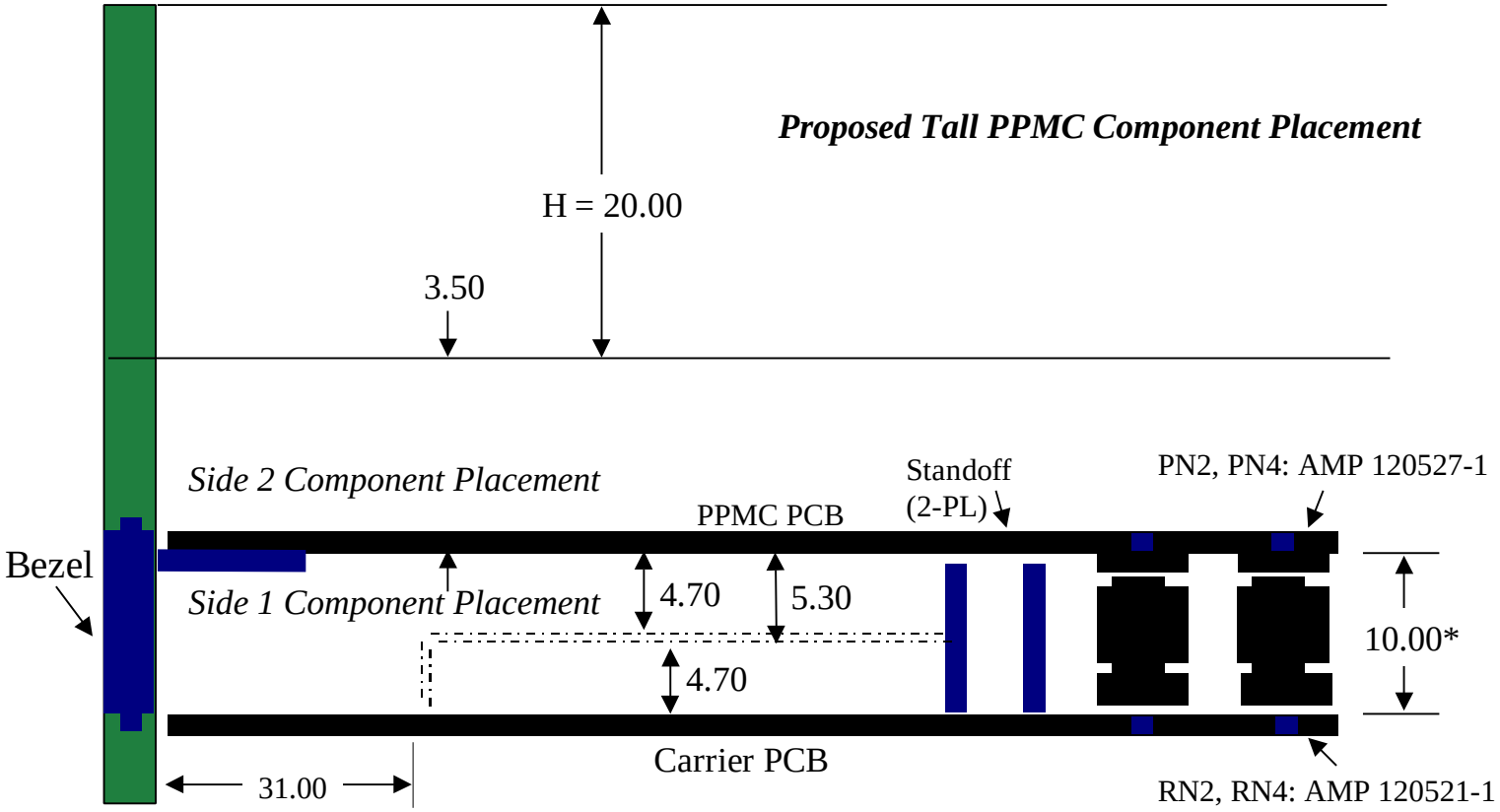
5.3 Signaling Voltage Levels~~Mapping of PCI Reserve Pins~~

Observation: Signaling voltage levels of PPMC must be compatible with PCI bus signals. Therefore if a PPMC is installed on a 3.3V PCI bus, make sure that 3.3V and not 5V signal levels are used.~~*No change from IEEE P1386.1*~~

~~6~~Mechanical Specifications

The PPMC retains width and length standards specified by the IEEE 1386 specification, adding a new height allowance option. Refer to Figure 1 for a summary of the standard and tall options for PPMCs.

Figure 1: Side View of Proposed Processor PMC, Standard & Tall



All units are in millimeters (mm)
Not to scale * = 10 mm recommended height